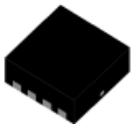
AccuPower 0.4~2 A Adjustable Over-Current Protection Load Switches

FPF2700, FPF2701, FPF2702



Top View

Bottom View

WDFN8 3x3, 0.65P
MLP
CASE 511DD

Top View

SOIC8
SO8
CASE 751EB

Description

The AccuPower FPF270X series is a family of current−limit load switches that provide full protection to systems and loads from excess current conditions. Minimum current limit is adjustable from 0.4 A to 2.0 A. The FPF270X contains a slew−rate−controlled N−channel MOSFET and slew−rated turn−on to prevent power bus disturbances from being caused by “hot plugging” loads or momentary excess load demands. The input voltage range is 2.8 V to 36 V. Loads can be activated or deactivated with a low−voltage logic−compatible ON pin. Fault conditions can be monitored using the error flag pin and/or the power−good pin.

Each member of the FPF270X family serves a category of load−fault response. All devices clamp the load current so that it cannot exceed an externally programmed current level. An over temperature feature provides further device protection in case of excessive levels of power dissipation.

FPF2700 responds to an overload condition that lasts longer than a fixed blanking period by turning off the load, followed by a retry after the auto−restart time.

FPF2701 responds to an overload condition that lasts longer than a fixed blanking period by latching off the load. The load remains off unless either the ON pin is toggled or the input voltage cycles through UVLO.

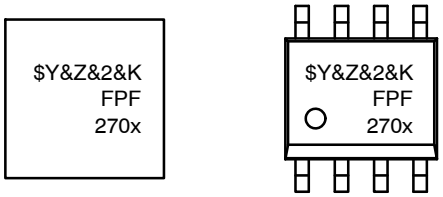
FPF2702 is intended to be used with external fault management. Like the FPF2700 and FPF2701, it sets the fault signal pin LOW when it activates current clamping. This device is intended for applications where external fault management coordinates the overload response with the FPF2702.

The FPF270X is available in a space−saving, Lead and Halogen free, 8−lead, MLP 3x3 mm and SO8 packages.

Features

- 2.8 V to 36 V Input Voltage Range
- Typical $R_{DS(ON)}$ = 88 mΩ
- 0.4 A to 2 A Adjustable Current Limit (Min.)
- Slew Rate Controlled
- ESD Protected, Above 2000 V HBM
- Thermal Shutdown
- Active LOW Enable
- UVLO Protection
- Power−Good Output
- These are Pb−Free Devices

MARKING DIAGRAM



WDFN8 SOIC8

FPF270x = Device Code (x = 0, 1, 2)
$Y = Logo
&Z = Assembly Plant Code
&2 = 2−Digit Date Code
&K = 2−Digits Lot Run Traceability Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 17 of this data sheet.

Applications

- Motor Drives
- Digital Cameras
- Consumer Electronics
- Industrial
- Computing
- Hard Disk Drives
- Telecom Equipment

APPLICATION DIAGRAM

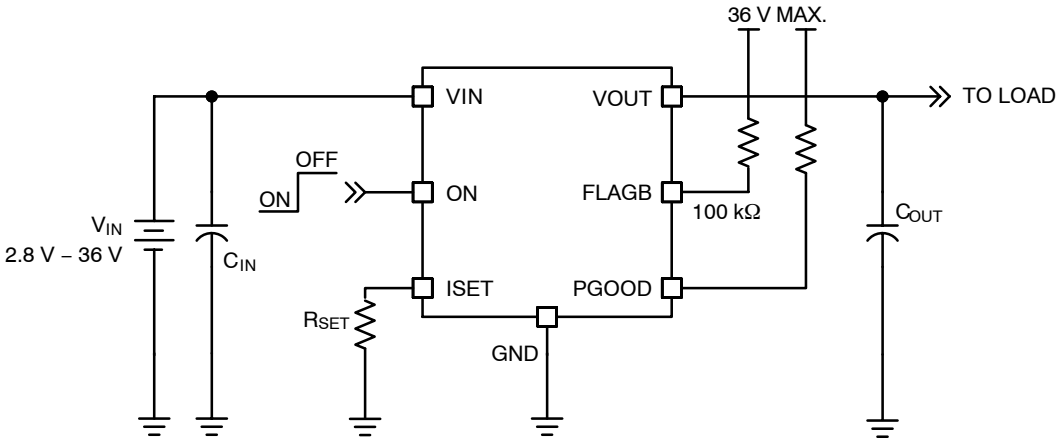


Figure 1. Typical Application

BLOCK DIAGRAM

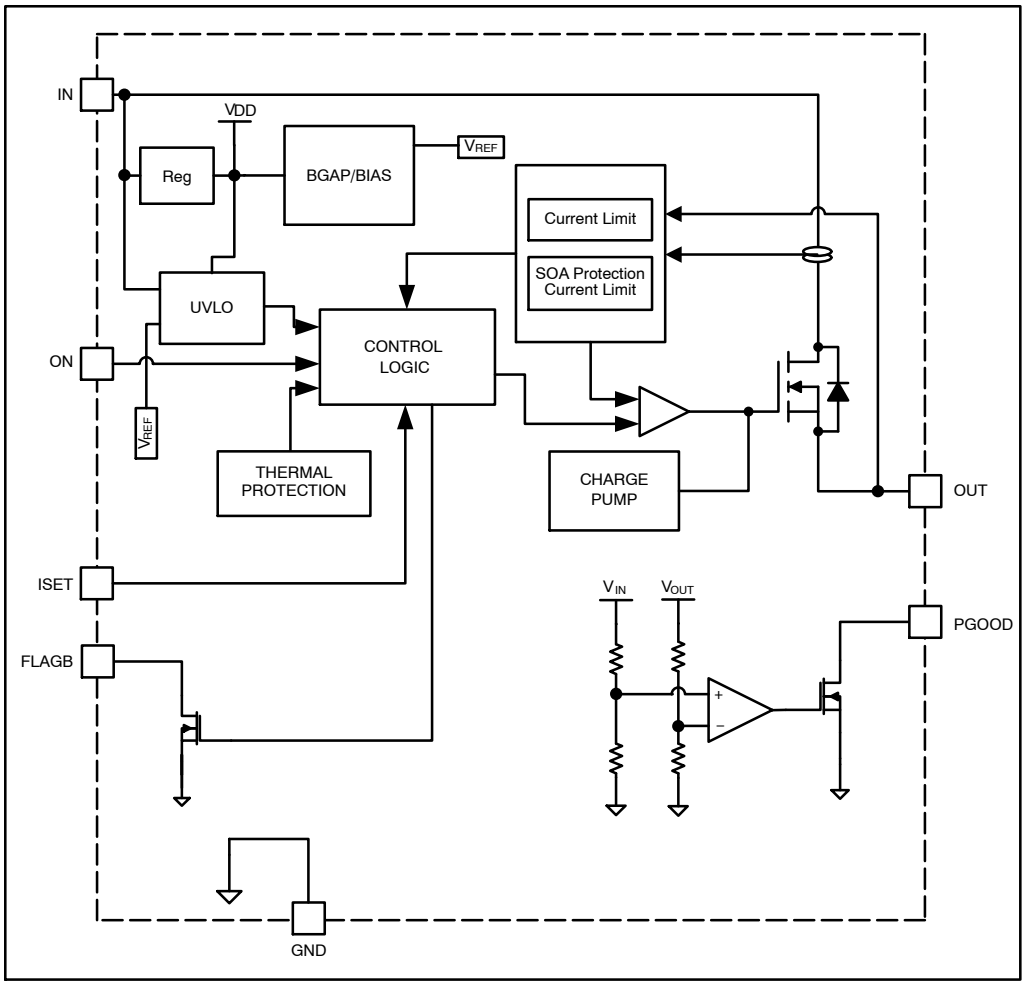


Figure 2. Block Diagram

PIN CONFIGURATIONS

PIN DEFINITIONS

Pin No.	Name	Description
1	VIN	Supply Input. Input to the power switch and the supply voltage for the IC.
2	PGOOD	Power−Good Output. Open−drain output to indicate that output voltage has reached 90% of input voltage.
3	ISET	Current Limit Set Input. A resistor from ISET to ground sets the current limit for the switch.
4	ON	ON Control Input. Active LOW.
5	GND	Ground
6	NC	No connection. Leave open or connect to ground.
7	FLAGB	Fault Output. Active LOW, open−drain output that indicates current limit, under−voltage, or over−temperature state.
8	VOUT	Switch Output. Output of the power switch.

MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
	PGOOD, FLAGB, VIN to GND		−0.3	40	V
	VOUT to GND		−0.3	V_{IN} + 0.3	V
	ON to GND		−0.3	6	V
P_D	Power Dissipation (T_A = 25°C)	MLP 3x3 (Note 1), *See Figure 3*	–	1.25	W
		SO8 (Note 1), *See Figure 5*	–	1.00	
I_{SW}	Maximum Continuous Switch Current		–	3.5	A
T_J	Operating Junction Temperature		−40	+125	°C
T_{STG}	Storage Temperature		−65	+150	°C
ESD	Electrostatic Discharge Protection Level	Human Body Model, JESD22−A114	2000	–	V
		Charged Device Model, JESD22−C101	2000	–	
Θ_{JA}	Thermal Resistance, Junction to Ambient	MLP 3x3 (Note 1), *See Figure 3*	–	80	°C/W
		SO8 (Note 1), *See Figure 5*	–	102	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Thermal resistance, θ_{JA}, is determined with the device mounted on a one inch square pad, 2 oz copper pad, and a 1.5 x 1.5 in. board of FR−4 material.

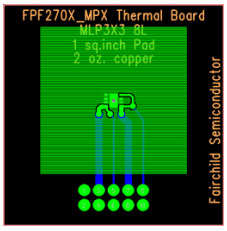


Figure 3. 80°C/W Mounted on a 1in^2 Pad of 2−oz. Copper

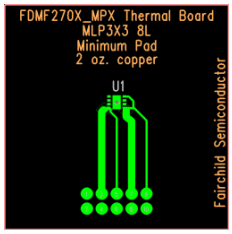


Figure 4. 226°C/W Mounted on a Minimum Pad of 2−oz. Copper

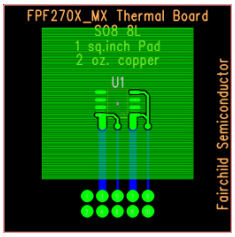


Figure 5. 102°C/W mounted on a 1in^2 Pad of 2−oz. Copper

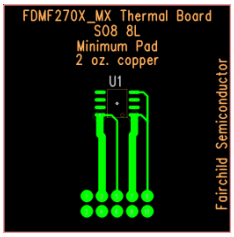


Figure 6. 181°C/W Mounted on a Minimum Pad of 2−oz. Copper

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{IN}	Input Supply Voltage	2.8	36.0	V
T_A	Ambient Operating Temperature	−40	85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

ELECTRICAL CHARACTERISTICS (V_{IN} = 2.8 to 36 V and T_A = −40 to +85°C unless otherwise noted. Typical values are at V_{IN} = 12 V and T_A = 25°C.)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
BASIC OPERATION						
V_{IN}	Operating Voltage		2.8		36.0	V
I_Q	Quiescent Current	V_{IN} = 12 V, V_{ON} = 0 V, I_{OUT} = 0 A	–	92	140	μA
I_{SHDN}	Shutdown Current	V_{IN} = 36 V, V_{ON} = 3.3 V, I_{OUT} = 0 A	–	5	14	μA
R_{ON}	On Resistance	T_A = 25°C, V_{IN} = 12 V	–	88	114	mΩ
		T_A = −40 to +85°C, V_{IN} = 12 V	–	–	140	
		T_A = 25°C, V_{IN} = 5 V	–	88	114	
		T_A = −40 to +85°C, V_{IN} = 5 V	–	–	140	
V_{IH}	ON Input Logic HIGH Voltage	V_{IN} = 2.8 to 36 V	2.0	–	–	V
V_{IL}	ON Input Logic LOW Voltage	V_{IN} = 2.8 to 36 V	–	–	0.8	V
I_{LK}	ON Input Leakage	V_{ON} = 5.5 V or GND	–1	–	1	μA
I_{SWOFF}	Off Switch Leakage	V_{IN} = 36 V, V_{ON} = 3.3 V, V_{OUT} = 0 V	–	0.01	–	μA
$V_{FLAGB(LO)}$	FLAGB Output Logic LOW Voltage	V_{IN} = 5 V, I_{SINK} = 1 mA	–	0.1	0.2	V
$I_{FLAGB(HI)}$	FLAGB Output Logic HIGH Leakage Current	V_{IN} = 36 V, Switch On, V_{FLAGB} = 36 V	–	–	1	μA
V_{PGOOD}	PGOOD Trip Voltage	V_{IN} = 5 V, V_{OUT} as Percent of V_{IN}, V_{OUT} Rising	–	90	–	%
$V_{PGOOD(HYS)}$	PGOOD Hysteresis	V_{IN} = 5 V, V_{OUT} as Percent of V_{IN}, V_{OUT} Falling	–	3	–	%
$V_{PGOOD(LO)}$	PGOOD Output Logic LOW Voltage	V_{IN} = 5 V, I_{SINK} = 1 mA	–	0.1	0.2	V
$I_{PGOOD(HI)}$	PGOOD Output High Leakage Current	V_{IN} = 36 V, Switch ON, V_{PGOOD} = 36 V	–	–	1	μA
PROTECTIONS						
I_{LIM}	Current Limit	T_A = 25°C	–20	–	+20	%
I_{SC}	Short Circuit Current Limit	V_{OUT} < 2 V, Switch in Over−Current Condition	–	0.75 x I_{NOM}	–	A
TSD	Thermal Shutdown	Shutdown Threshold	–	140	–	°C
		Return from Shutdown	–	110	–	
		Hysteresis	–	30	–	
UVLO	Under−Voltage Shutdown	V_{IN} Increasing	2.3	2.5	2.7	V
UVLO_HYST	Under−Voltage Shutdown Hysteresis		–	100	–	mV
DYNAMIC						
t_{don}	Turn On Delay	R_L = 500 Ω, C_L = 2 μF	–	2.7	–	ms
t_{doff}	Turn Off Delay		–	0.1	–	
t_R	V_{OUT} Rise Time		–	7.5	–	
t_F	V_{OUT} Fall Time		–	1.5	–	
t_{BLANK}	Over−Current Blanking Time	FPF2700/1, T_A = 25°C	0.25	0.50	0.75	ms
$t_{RESTART}$	Auto−Restart Time	FPF2700, T_A = 25°C	63.8	127.5	191.2	ms
t_{CLR}	Current−Limit Response Time	V_{IN} = 12 V, V_{ON} = 0 V	–	50	–	μs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

TIMING DIAGRAM

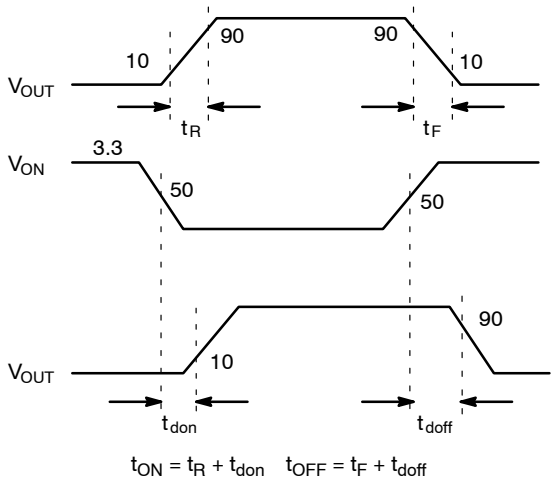


Figure 7. Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

(V_{IN} = 12 V and T_A = 25°C)

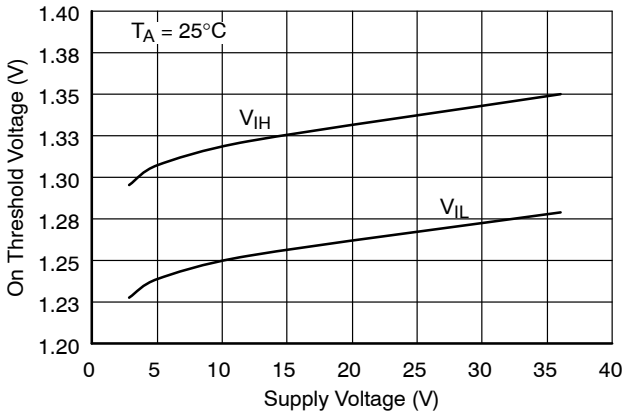


Figure 8. ON Threshold vs. Supply

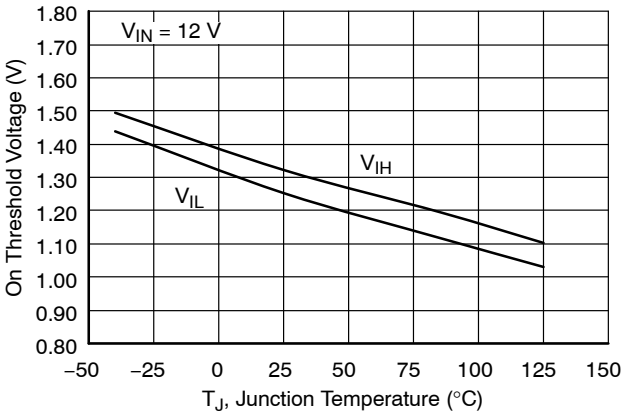


Figure 9. ON Threshold vs. Temperature

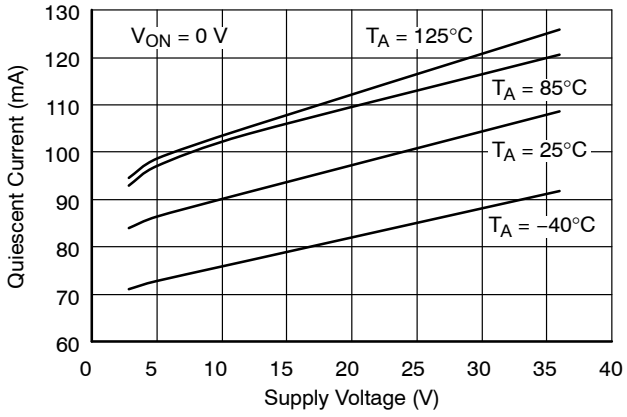


Figure 10. Quiescent Current vs. Supply Voltage (ON)

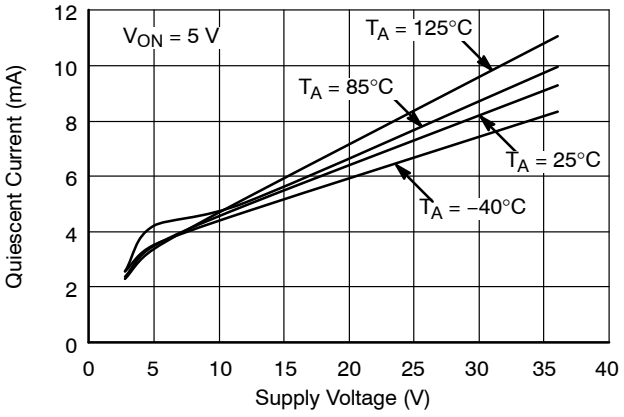


Figure 11. Quiescent Current vs. Supply Voltage (OFF)

TYPICAL PERFORMANCE CHARACTERISTICS

(V_{IN} = 12 V and T_A = 25°C) (continued)

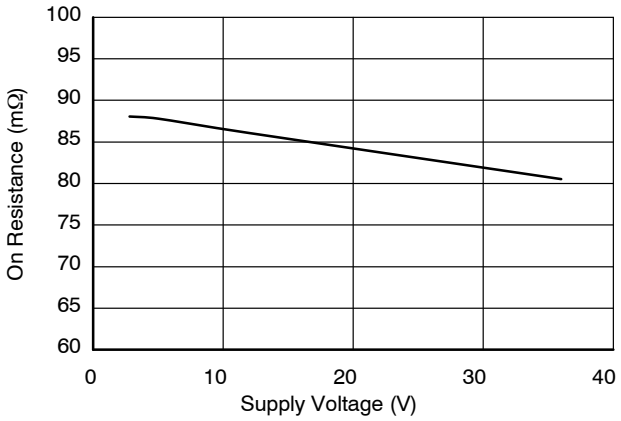


Figure 12. On Resistance vs. Supply Voltage

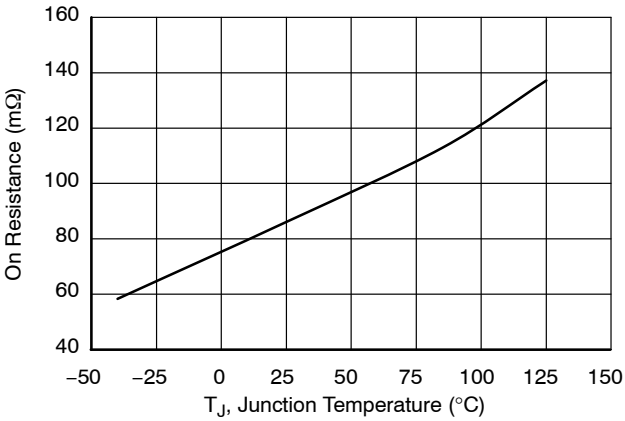


Figure 13. On Resistance vs. Junction Temperature

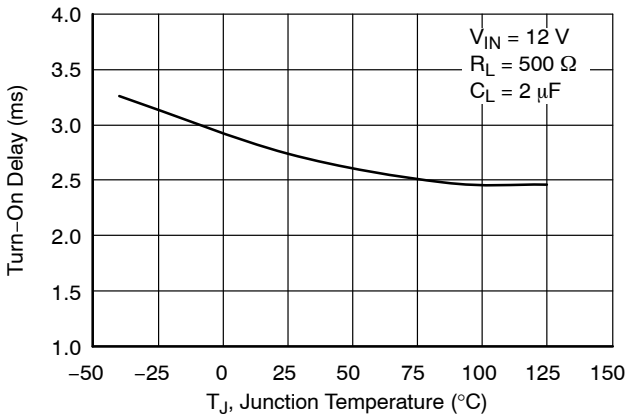


Figure 14. Turn−On Delay vs. Junction Temperature

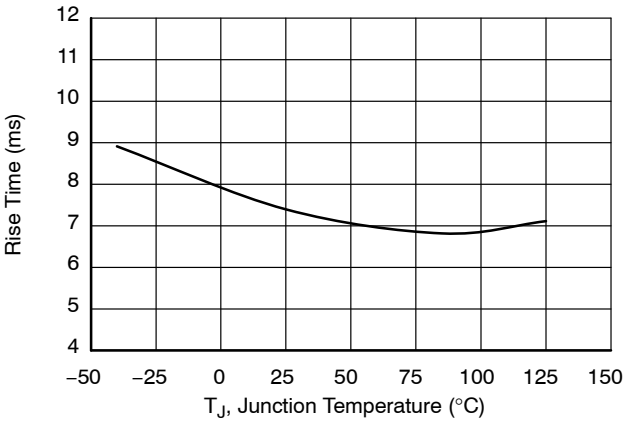


Figure 15. Output Rise Time vs. Junction Temperature

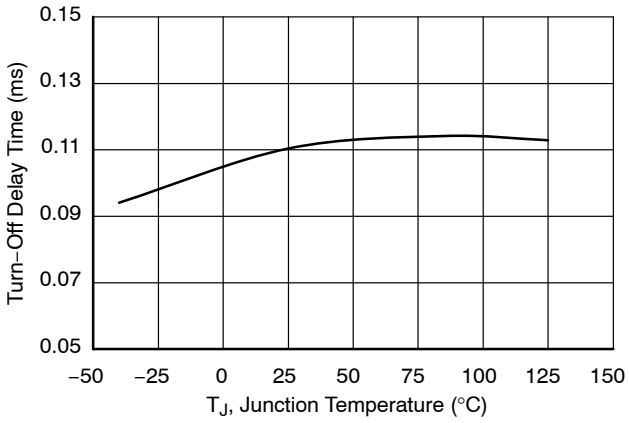


Figure 16. Turn−Off Delay vs. Junction Temperature

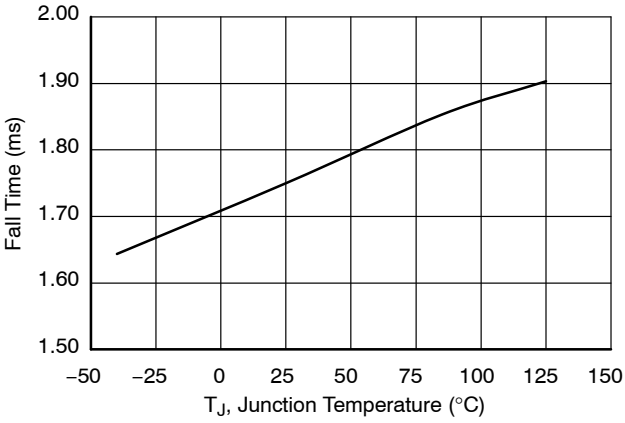


Figure 17. Output Fall Time vs. Junction Temperature

TYPICAL OPERATION CHARACTERISTICS OF FPF2700 AND FPF2701

(When V_{OUT} < 2 V, the current limit is set to 75% of I_{LIM})

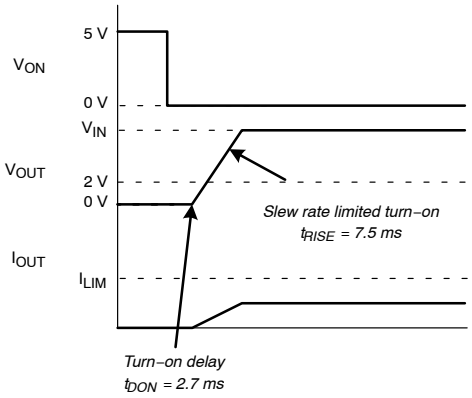


Figure 18. Normal Startup to 0.5X I_{LIM}

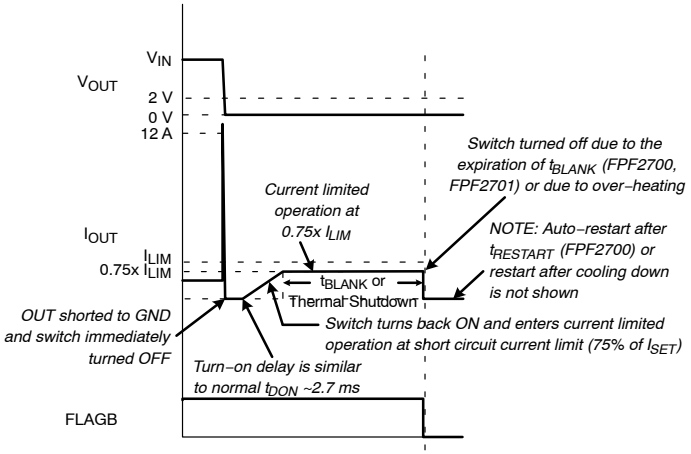


Figure 19. OUT Shorted to GND, Short Condition Persists (SOA Protection Followed by Current−Limited Operation)

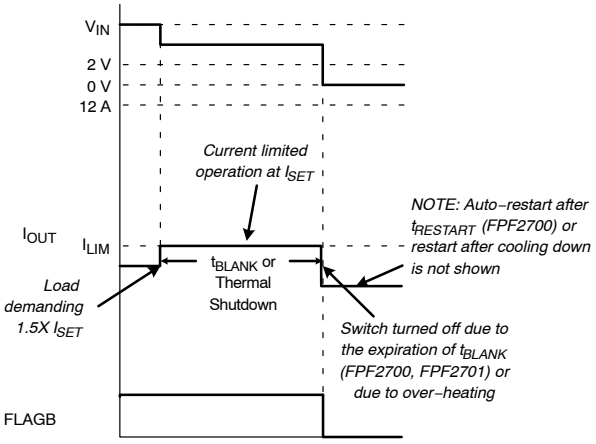


Figure 20. OUT Overloaded with 1.5X I_{LIM} (Long−Duration Overload)

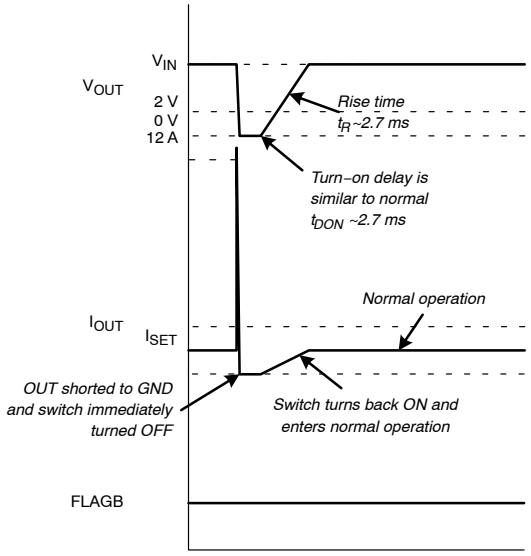


Figure 21. OUT Shorted to GND, Short Condition Removed (SOA Protection Followed by Normal Operation)

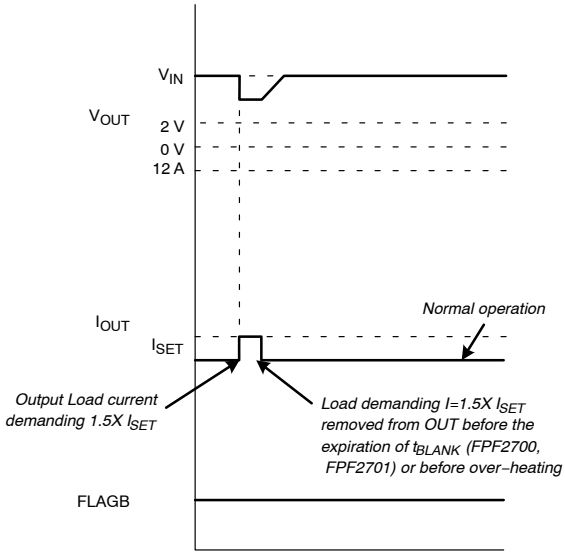


Figure 22. OUT Overloaded with 1.5X I_{LIM} (Transient Overload)

TYPICAL OPERATION CHARACTERISTICS OF FPF2702

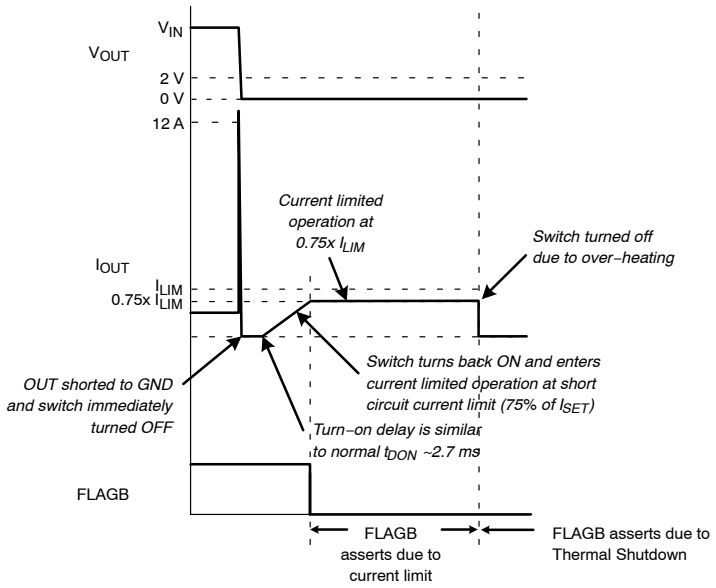


Figure 23. OUT Shorted to GND, Short Condition Persists (SOA Protection Current Limit Followed by Current Limit)

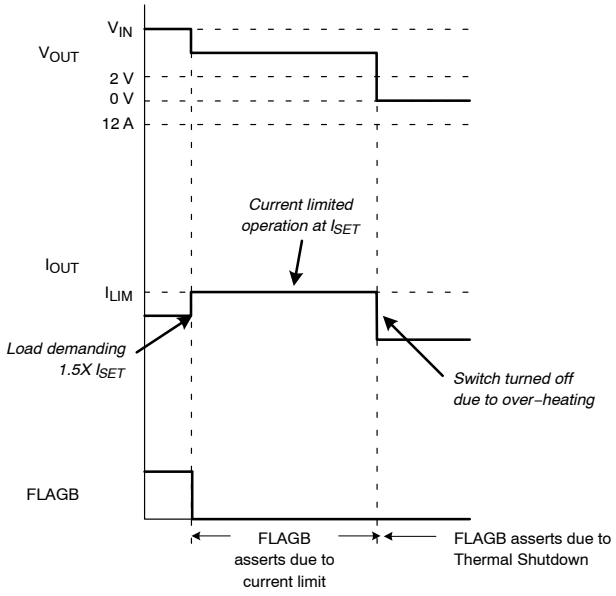


Figure 24. OUT Overloaded with 1.5X I_{LIM} (Long−Duration Overload)

TYPICAL PERFORMANCE CHARACTERISTICS FPF270X

(V_{IN} = 12 V and T_A = 25°C)

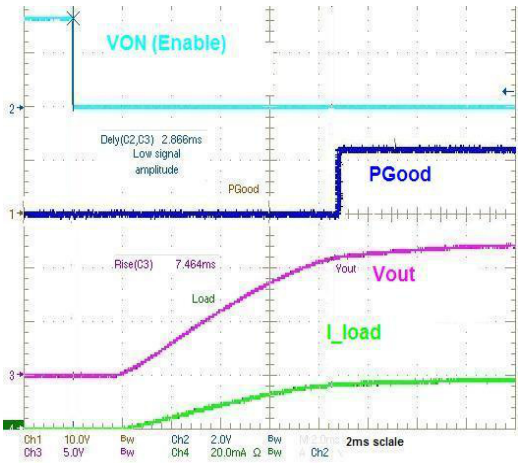


Figure 25. 12 V Turn−On Delay (R_L = 500 Ω, C_{OUT} = 2 μF)

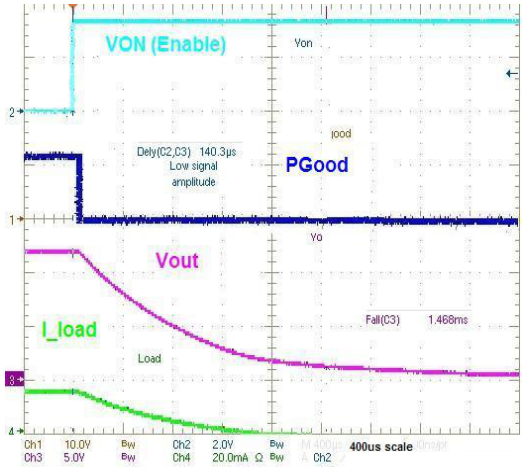


Figure 26. 12 V Turn−Off Delay (R_L = 500 Ω, C_{OUT} = 2 μF)

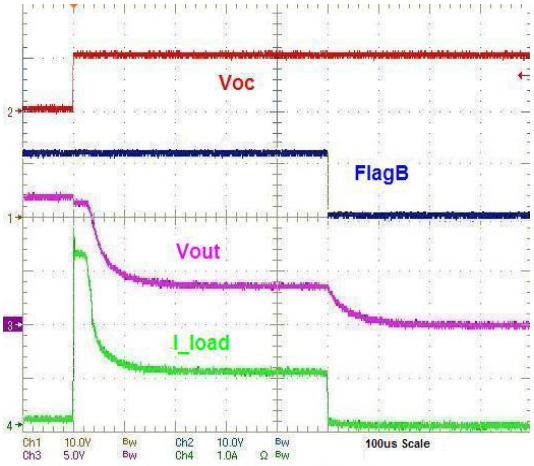


Figure 27. 12 V Blanking Time (Output Overloaded and t_{blank} Expired, FPF2700/01, I_{LIM} = 1 A, I_{LOAD} = 3.3 A, C_{OUT} = μF, R_{LOAD} = 500 W) V_{OC} (Note 2)

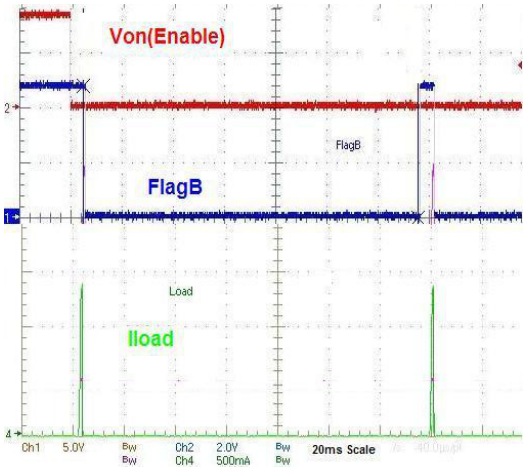


Figure 28. Restart Time (Switch Turned ON into Persistent Over−Current Condition, $t_{RESTART}$~127.5 ms)

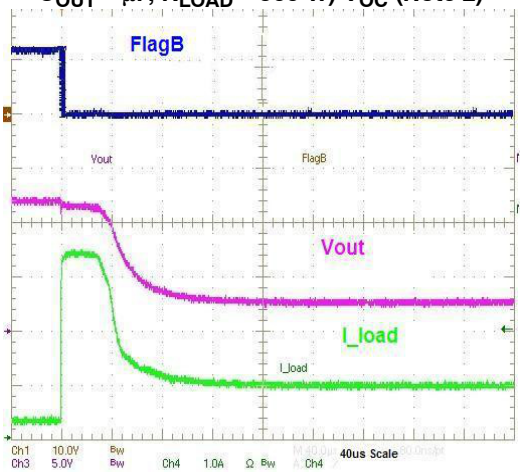


Figure 29. Soft Overload and Constant Current (I_{LOAD} > I_{LIM}, FPF2702 Enters Constant Current Mode, Running at I_{LIM})

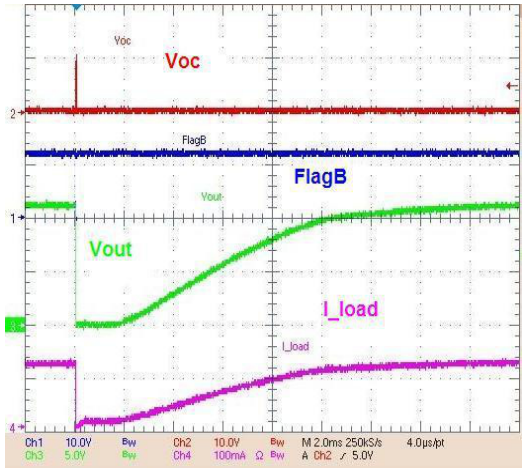


Figure 30. OUT Shorted to GND, Short Condition Removed (SOA Protection Followed by a Normal Operation, FPF2700 / FPF2701)

NOTE:

2. V_{OC} signal forces the device into an over−current condition by loading a 500 mΩ resistor to the output through an NMOS. V_{OC} is the gate drive of the NMOS.

APPLICATION INFORMATION

Description of Operation

The FPF270X family of current limit load switches is designed to meet the power requirements of a variety of applications with wide input voltage range of 2.8 V to 36 V and adjustable current−limit value. The FPF270X family offers control and protection while providing optimum operation current for safe design practices. The core of each switch is a typical 88 mΩ (V_{IN} = 12 V) N−channel MOSFET and a controller capable of functioning over an input voltage range of 2.8 V to 36 V.

FPF270X offers adjustable current limiting, under−voltage lockout (UVLO), power−good indicator (PGOOD), fault flag output (FLAGB), and thermal shutdown protection. In the event of an over−current condition, the load switch limits the load to the current limit value. The current limit value for each switch can be adjusted from 400 mA to 2 A through the ISET pin.

On/Off Control

The ON pin is active LOW for and controls the state of the switch. Pulling the ON pin continuously to LOW holds the switch in ON state. The switch moves into OFF state when the ON pin is pulled HIGH. The ON pin can be pulled HIGH to a maximum voltage of 5.5 V.

An under−voltage condition on the input voltage or a junction temperature in excess of 140°C overrides the ON control and turns off the switch. In addition, an over− current condition causes the switch to turn off in the FPF2700 and FPF2701 after the expiration of the blanking time. The FPF2700 has an auto−restart feature that automatically turns the switch ON again after the auto−restart time. For the FPF2701, the ON pin must be toggled to turn the switch on again. The FPF2702 does not turn off in response to an over−current condition; it remains operating in Constant−Current Mode as long as ON is enabled and the thermal shutdown or UVLO have not activated. The ON pin does not have internal pull−down or pull−up resistors and should not be left floating.

Fault Reporting

Upon detection of an over−current condition, an input UVLO, or an over−temperature condition, the FLAGB signals the Fault Mode by activating LOW. In the event of an over−current condition for the FPF2700 or FPF2701, the FLAGB goes LOW at the end of the blanking time (Figure 19 and Figure 20). FLAGB goes LOW immediately for the FPF2702 (Figure 24). If the over−current condition lasts longer than blanking time, FLAGB remains LOW through the auto−restart time for the FPF2700. For the FPF2701, FLAGB is latched LOW and ON must be toggled to release it.

For FPF2702, FLAGB is LOW during a fault and immediately returns HIGH at the end of the fault condition. FLAGB is an open−drain MOSFET that requires a pull−up resistor. The maximum pull−up voltage is 36 V (Figure 24).

During shutdown, the pull−down on FLAGB is disabled to reduce current draw from the supply. A 100 kΩ pull− up resistor is recommended in the application.

Current Limiting

The current limit ensures that the current through the switch doesn't exceed a maximum value while not limiting at less than a minimum value. The current−limit level is adjustable through an external resistor connected between the ISET pin and GND.

The typical current limit level is adjustable from 510 mA to 2.5 A. The minimum current limit ($I_{LIM(MIN)}$) range is from 0.4 A to 2.0 A, including 20% current−limit tolerance. The FPF2700 and FPF2701 have a blanking time during which the switch acts as a constant−current source (Figure 22). If the over−current condition persists beyond the blanking time, the FPF2700 latches off and shuts the switch off (Figure 27). If the ON pin is kept active, an auto−restart feature releases the switch and turns the switch on again after the auto−restart time (Figure 28). If the over−current condition persists beyond the blanking time, the FPF2701 latch−off feature shuts the switch off. The switch is kept off until the ON pin is toggled or input power is cycled. The FPF2702 has no current−limit blanking period, so it remains in a constant−current state until the ON pin is deactivated or the thermal shutdown turns off the switch.

Besides the current−limiting functionality, the switch is protected by the thermal shutdown protection and an independent SOA protection circuit is available.

SOA Protection Current Limit (I_{OUT} > 12 A)

FPF270X has an SOA protection feature to protect the load switch in response to current surges exceeding 12 A in normal operation. If a short−circuit event occurs (I_{OUT} > 12 A), the switch is turned off in about 1 μs by an independent Safe Operating Area (SOA) protection circuit (Figure 21, Figure 23). This feature protects the switch in case of sudden, high−current events at the output, such as a short to GND. The switch turns on automatically after a turn−on delay of about 2.7 ms.

Short−Circuit Current Limit (V_{OUT} < V_{SCTH} = 2 V)

When the output voltage drops below the short−circuit threshold voltage, V_{SCTH}, the current−limit value reconditions itself to the short−circuit current limit value, which is 75% of the nominal current limit (0.75 x $I_{LIM,}$) (Figure 19). This prevents early thermal shutdown by reducing the power dissipation of the device. The V_{SCTH} value is set at 2 V. At about V_{OUT} = 2.1 V, the switch is removed from short−circuit current−limiting mode and the current limit is set to the nominal current limit value.

Setting the Current Limit Value

FPF270X has an adjustable 0.4 A to 2.0 A minimum current limit set through an external resistor, R_{SET}, connected between ISET and GND. A precision R_{SET} value must be used, such as 1% tolerance or lower, to minimize the total current limit tolerance of the system.

Use the following equation to calculate the value of the resistor for intended typical current limit value:

$$R_{SET}\ (k\Omega) = \frac{277.5}{I_{LIM(TYP)}\ (A)} \qquad \text{(eq. 1)}$$

$I_{LIM(TYP)}$ is the typical current limit value based on a R_{SET}.

Table 1. R_{SET} SELECTION GUIDE

	Current Limit (A)			
R_{SET} (kΩ)	Min	Typ	Max	Tol. (%)
111	2.00	2.50	3.00	20
124	1.79	2.24	2.69	20
147	1.51	1.89	2.27	20
182	1.22	1.52	1.83	20
220	1.01	1.26	1.51	20
274	0.81	1.01	1.22	20
374	0.59	0.74	0.89	20
549	0.40	0.51	0.61	20

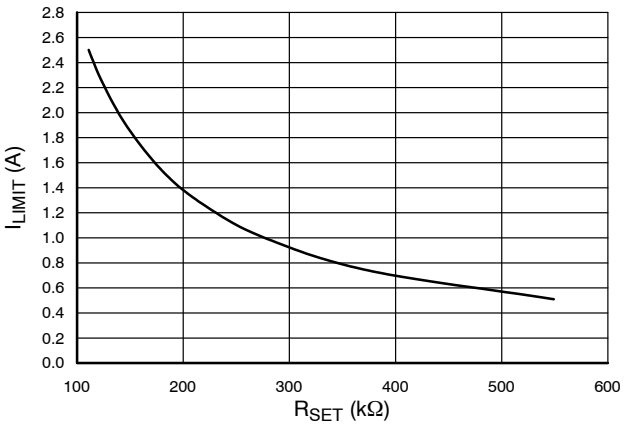


Figure 31. I_{LIM} vs. R_{SET}

Under−Voltage Lockout (UVLO)

The under−voltage lockout feature turns off the switch if the input voltage drops below the under−voltage lockout threshold. With the ON pin active (ON pin pulled LOW), the input voltage rising above the under−voltage lockout threshold causes a controlled turn−on of the switch (Figure 32). The UVLO threshold voltage is set internally

at 2.5 V for V_{IN} rising. The under−voltage lockout threshold has a 0.1 V hysteresis.

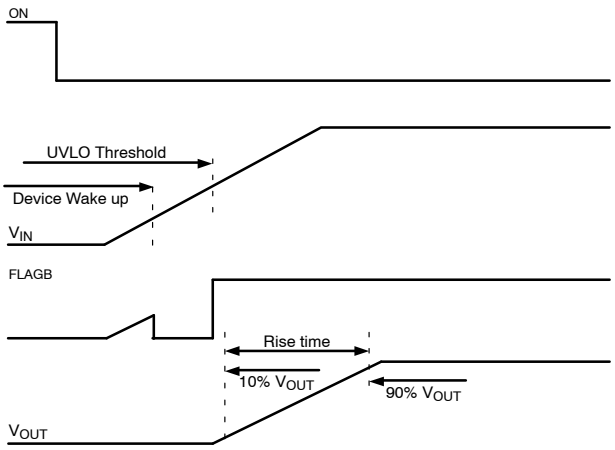


Figure 32. Under−Voltage Lockout Performance

Power Good

FPF270X has a power good feature. The PGOOD pin is an open−drain MOSFET that asserts HIGH when the output voltage reaches 90% of the input voltage (Figure 21). A typical 3% PGOOD hysteresis is added to PGOOD to prevent PGOOD from chattering as V_{OUT} falls near the PGOOD threshold voltage.

The PGOOD pin requires an external pull−up resistor connected to an external voltage source compatible with input levels of other chips connected to this pin. PGOOD is kept LOW when the device is inactive. To save current in the OFF state, the pull−up resistor of the PGOOD pin can be connected to the output voltage when there is no battery, provided that compatibility with the input levels of other devices connected to PGOOD is observed. A typical value of 100 kΩ is recommended for the pull up resistor. When the power−good feature is not used in the application, the PGOOD pin can be connected to GND.

Thermal Shutdown

Thermal shutdown protects the die from internally or externally generated excessive temperatures. During an over−temperature condition; as the temperature increases above 140°C, FLAGB is activated and the switch is turned off.

When the die cools down sufficiently (die temperature drops below the threshold level), the switch automatically turns on again. To avoid unwanted thermal oscillations, a 30°C (typical) thermal hysteresis is implemented between thermal shutdown entry and exit temperatures. Proper board layout is required to prevent premature thermal shutdown *(see Figure 33 for thermal shutdown behavior on FPF2702)*.

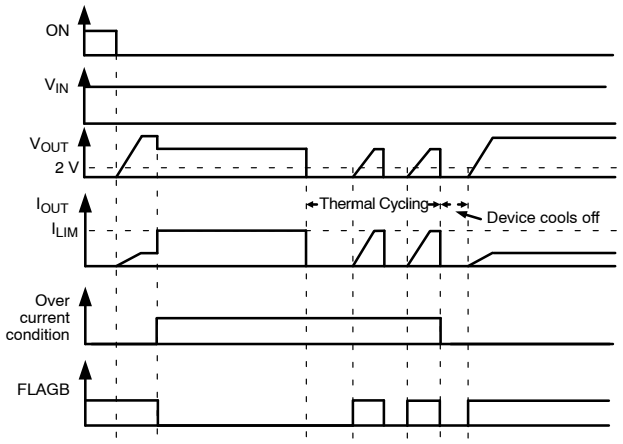


Figure 33. FPF2702 Thermal Shutdown Behavior

SOA (FPF2702)

During extended output−short conditions, excessive power dissipation occurs in the load switch. FPF2700 and PFP2701 are protected by turning off the load switch after blanking time. FPF2702 has no blanking time feature; please refer to Note 3.

It is possible to estimate the SOA for the two FPF2702 packages, MPX and MX, through their respective SOA curves shown in Figure 34 and Figure 35. These curves provide a reference on how long the load switch survives under the worst−case scenario with minimum pad size of one square inch. (Note 1)

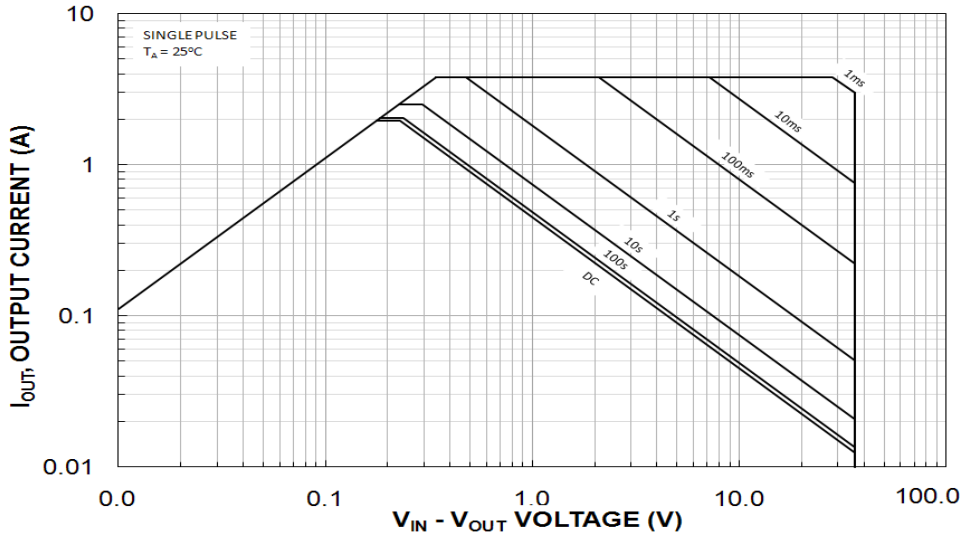


Figure 34. FPF2702 MPX SOA

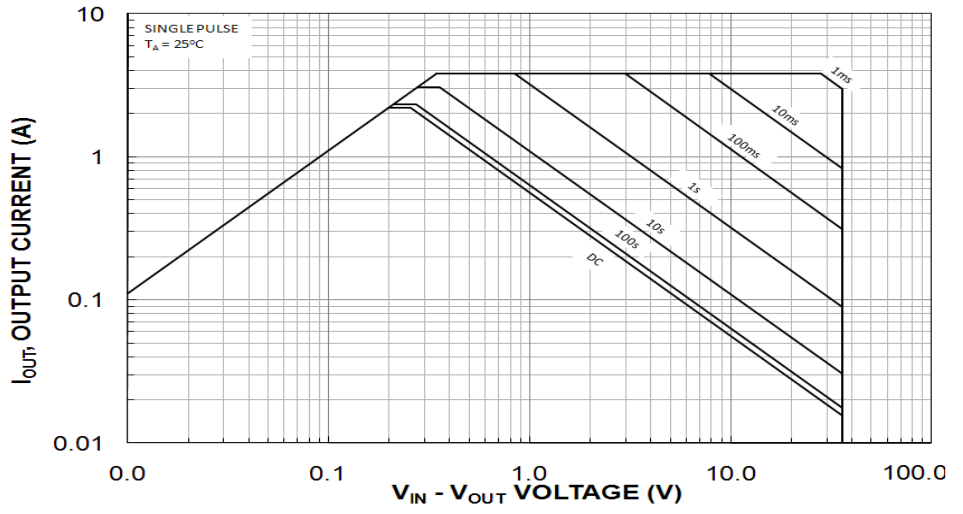


Figure 35. FPF2702 MX SOA

NOTE:

3. To protect FPF2702 from an extended short condition, additional protection must be implemented in the system to protect the device. For example, the FLAGB and PGOOD signal can be used to monitor the short−circuit fault condition. In applications where FPF2702 can be exposed to persistent short−circuit conditions, it should be used only with external fault management control to protect the switch.

Input Capacitor

To limit the voltage drop on the input supply caused by transient inrush currents when the switch is turned on into a discharged load capacitor or short−circuit; an input capacitor, C_{IN}, is recommended between the IN and GND pins. The FPF270X features a fast current limit response time (50 μs). During this period, the device relies on the input capacitor to supply the load current. A 10 μF to 100 μF ceramic capacitor is adequate for C_{IN} in most cases. Larger C_{IN} values may be required in high−voltage or high−current applications. An electrolytic capacitor can be used in parallel to further reduce the voltage drop.

Output Capacitor

A 0.1 μF to 1 μF capacitor, C_{OUT}, should be placed between the OUT and GND pins. This capacitor helps prevent parasitic board inductances from forcing the output voltage below ground when the switch turns off. This capacitor should have a low dissipation factor. An X7R Multilayer Ceramic Chip (MLCC) capacitor is recommended.

During startup, the total output current consists of both the load current and the charge current of the output capacitor. For the FPF2700 and FPF2701; if the total output current exceeds the set current limit threshold (determined via R_{SET}) for longer than the blanking time, the device may not be able to start properly. This imposes an upper limit to the value of the output capacitor, given the load current and the selected current limit value. C_{OUT} should not exceed the C_{OUTmax} calculated in Equation 2 or the switch does not start properly due to the set current limit:

$$C_{OUTmax} \leq I_{LIM\_MIN} \times 500\ \mu s/V \quad \text{(eq. 2)}$$

High−Voltage Operation (Output Capacitor)

During a hard short condition on the output while operating at greater than 24 V V_{IN}, a large instantaneous inrush current is delivered to the shorted output. A capacitor must be placed at the OUTPUT pin, acting as a current source to support the instantaneous current draw (Table 2). A low−ESR capacitor is recommended. Once the value of the output capacitor is determined from Table 2, Equation 2 must be reevaluated.

Table 2. C_{OUT} SELECTION GUIDE

V_{IN} (V)	Capacitance (μF)
$24 < V_{IN} \leq 27$	22
$27 < V_{IN} \leq 32$	47
$32 < V_{IN} \leq 36$	68

Power Dissipation

During normal operation as a switch, the power dissipation of the device is small and has little effect on the operating temperature of the part. The maximum power dissipation for the switch in normal operation occurs just before the switch enters into current limit. This may be calculated using the equation:

$$P_{D\_MAX(NormalOperation)} = (I_{LIM(Max)})^2 \times R_{ON(MAX)} \quad \text{(eq. 3)}$$

The maximum junction temperature should be limited to 125°C under normal operation. Junction temperature can be calculated using the equation:

$$T_J = P_D \times \Theta_{JA} + T_A \quad \text{(eq. 4)}$$

where:

- T_J is junction temperature;
- P_D is power dissipation on the switch;
- Θ_{JA} is the thermal resistance, junction−to−ambient of the package; and
- T_A is ambient temperature.

Design Example

For a 12 V application and $I_{LIM\ (Max)}$ = 1 A, maximum power dissipation in a normal operation is calculated as:

$$P_{D\_MAX(NormalOperation)(VIN=12V)} = (1)^2 \times 0.140 = 140\ mW \quad \text{(eq. 5)}$$

FPF2702 $P_{D(Max)}$ during OC:

If device is in over−current condition and $V_{OUT} > 2$ V, power dissipation can be calculated as:

$$P_D = (V_{IN} - V_{OUT}) \times I_{LIM(Max)} \quad \text{(eq. 6)}$$

If device is in short−circuit current limit and $V_{OUT} < 2$ V, power dissipation can be calculated as:

$$P_D = (V_{IN} - V_{OUT}) \times (0.75 \times I_{LIM(Max)}) \quad \text{(eq. 7)}$$

Design Example:

Using FPF2702 in a V_{IN} = 5 V application where $I_{LIM\ (Max)}$ = 2 A, assuming V_{OUT} = 2.5 V; power dissipation across the switch is calculated as:

$$P_D = (5 - 2.5) \times 2 = 5\ W \quad \text{(eq. 8)}$$

Whereas in a short−circuit current−limit condition ($V_{OUT} \approx 0$ V), power dissipation is calculated as:

$$P_D = ((V_{IN} - V_{OUT}) \times (0.75 \times I_{LIM(Max)}) = (5 - 0) \times (0.75 \times 2) = 7.5\ W \quad \text{(eq. 9)}$$

PCB LAYOUT RECOMMENDATIONS

For the best performance, all traces should be as short as possible. To be most effective, the input and output capacitors should be placed close to the device to minimize the effects that parasitic trace inductances may have on normal and short−circuit operation (Figure 37). Using wide traces for IN, OUT, and GND pins helps minimize parasitic electrical effects as well as the case− to−ambient thermal impedance.

To minimize the interference between analog ground (chip ground, pin 5) and power ground during load current excursion, the ground terminal of the input and output capacitors and the R_{SET} resistor should be routed directly to chip ground and away from power ground.

Improving Thermal Performance

Improper layout could result in higher junction temperature and trigger thermal shutdown protection. This is particularly significant for the FPF2702, where the device operates in Constant Current Mode under overload conditions. During fault conditions, the power dissipation of the switch could exceed the maximum absolute power dissipation.

The following techniques improve the thermal performance of this family of devices. These techniques are listed in order of the significance of their impact.

1. Thermal performance of the load switch can be improved by connecting the Die Attach Pad (DAP) of the MLP 3x3 package to the GND plane of the PCB.
2. Embedding two exposed through−hole vias into the DAP provides a path for heat to transfer to the back GND plane of the PCB. A drill size of round, 15 mils (0.4 mm) with 1−ounce copper plating is recommended for appropriate solder reflow. A smaller−size hole prevents the solder from penetrating into the via, resulting in device lift−up. Similarly, a larger hole consumes excessive solder and may result in voiding the DAP.
3. The IN, OUT, and GND pins dissipate most of the heat generated during high−load current condition. The layout suggested in Figure 37 and Figure 38 is strongly recommended illustrating a proper layout for devices in MLP 3x3 packages. IN, OUT, and GND pins are connected to adequate copper so that heat may be transferred as efficiently as possible out of the device. The low−power FLAGB and ON pins traces may be laid−out diagonally from the device to maximize the area available to the ground pad. Place the input and output capacitors as close as possible to the device.

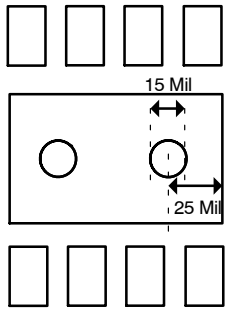


Figure 36. Two Through−Hole Open Vias Embedded in the DAP

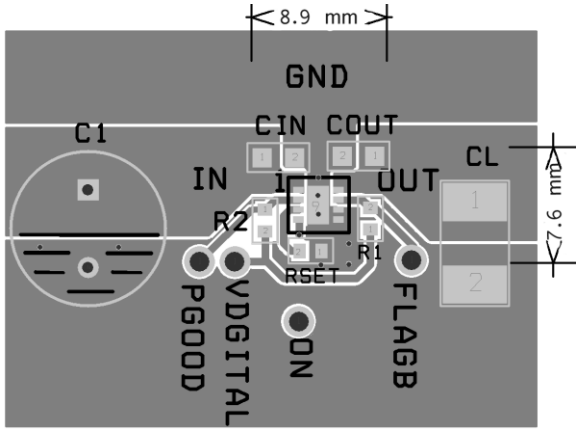


Figure 37. Proper Layout of Output and Ground Copper Area (Top, SST, and AST Layers)

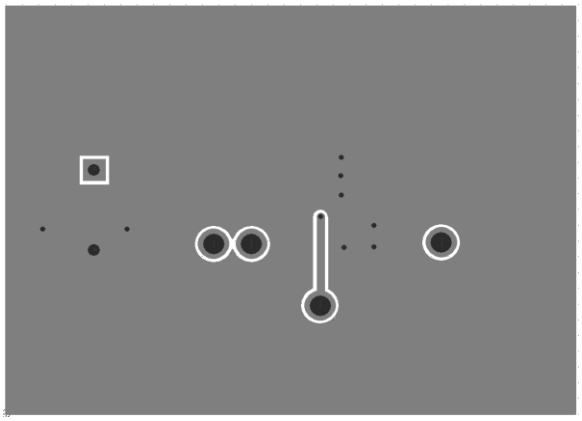


Figure 38. Proper Layout (Bottom and ASB Layers)

FPF270X DEMONSTRATION BOARD

The FPF270X demonstration board has components and circuitry to demonstrate the load switch's functions and features. Thermal performance of the board is improved using the techniques recommended in the layout recommendations section. Additional information about demonstration board can be found in the FPF270X board users guide.

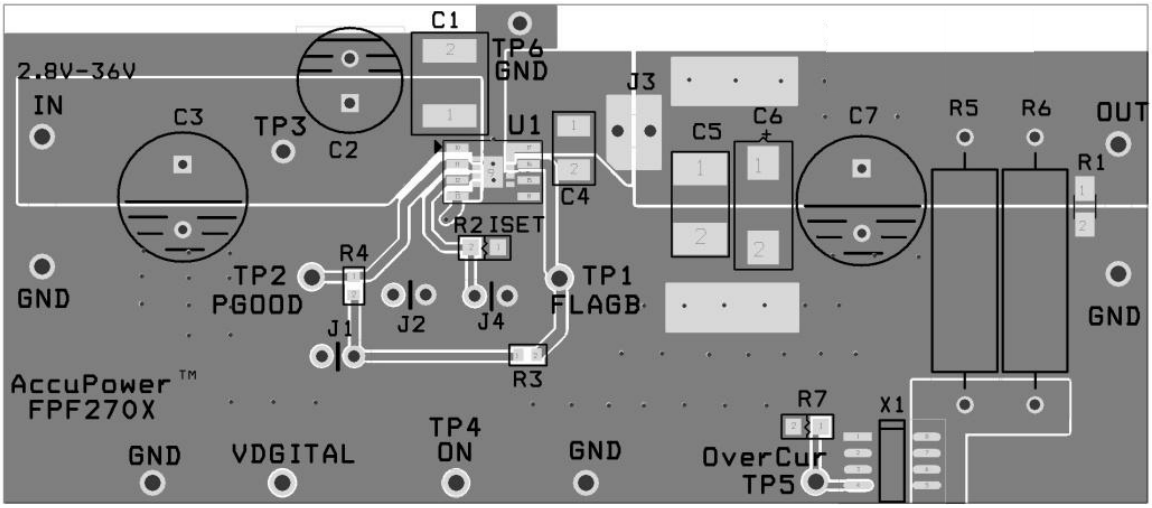


Figure 39. Top, SST, and AST Layers

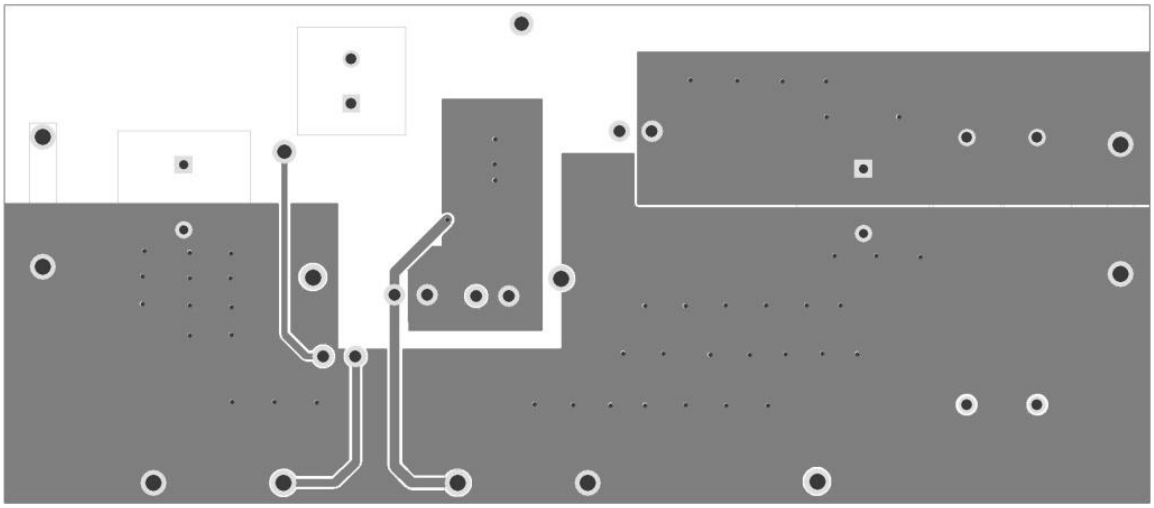


Figure 40. Bottom and ASB Layers

ORDERING INFORMATION

Part Number	Current Limit (A)	Current Limit Blanking Time (ms)	Auto−Restart Time (ms)	ON Pin Activity	Package	Shipping†
FPF2700MPX	0.4 – 2.0	0.5	127.5	Active LOW	WDFN8 3x3, 0.65P MLP3X3 (Pb−Free)	3000 / Tape & Reel
FPF2701MPX	0.4 – 2.0	0.5	NA	Active LOW	WDFN8 3x3, 0.65P MLP3X3 (Pb−Free)	3000 / Tape & Reel
FPF2702MPX	0.4 – 2.0	NA	NA	Active LOW	WDFN8 3x3, 0.65P MLP3X3 (Pb−Free)	3000 / Tape & Reel
FPF2700MX	0.4 – 2.0	0.5	127.5	Active LOW	SOIC8 SO8 (Pb−Free)	2500 / Tape & Reel
FPF2701MX	0.4 – 2.0	0.5	NA	Active LOW	SOIC8 SO8 (Pb−Free)	2500 / Tape & Reel
FPF2702MX	0.4 – 2.0	NA	NA	Active LOW	SOIC8 SO8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

WDFN8 3x3, 0.65P
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ISSUE O

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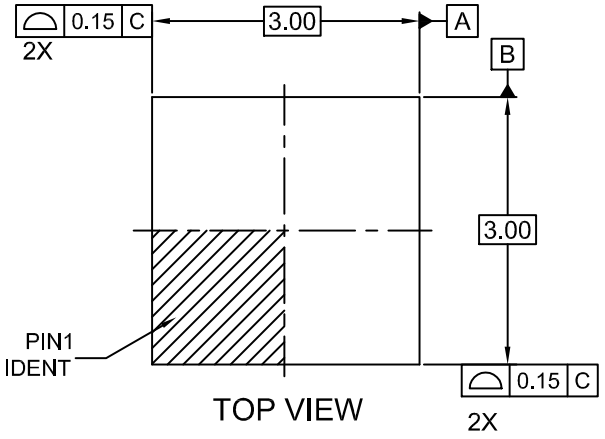
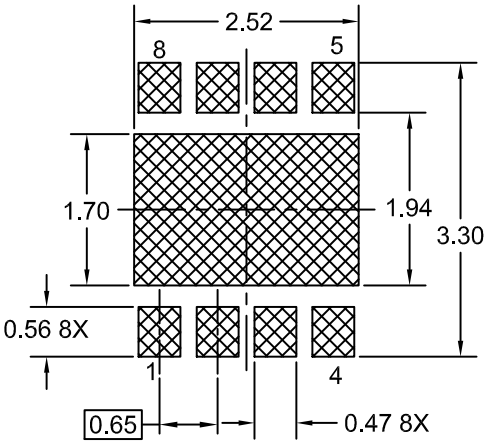


TOP VIEW



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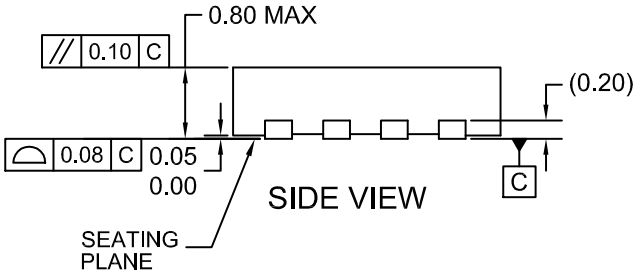

SIDE VIEW

NOTES:

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B. DIMENSIONS ARE IN MILLIMETERS.

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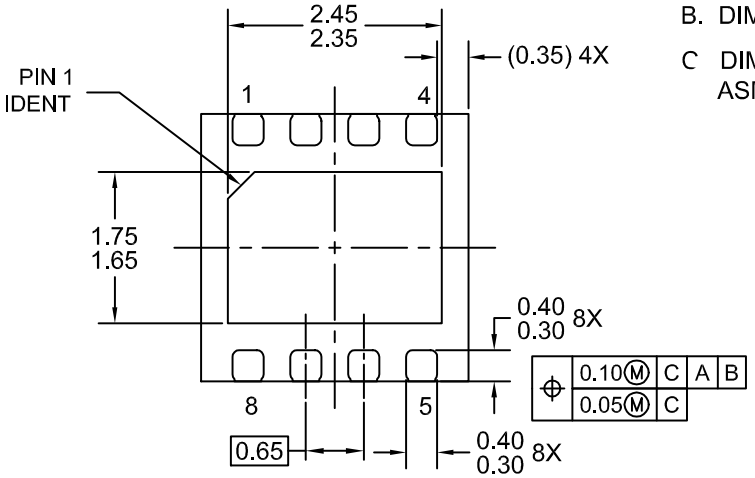

BOTTOM VIEW

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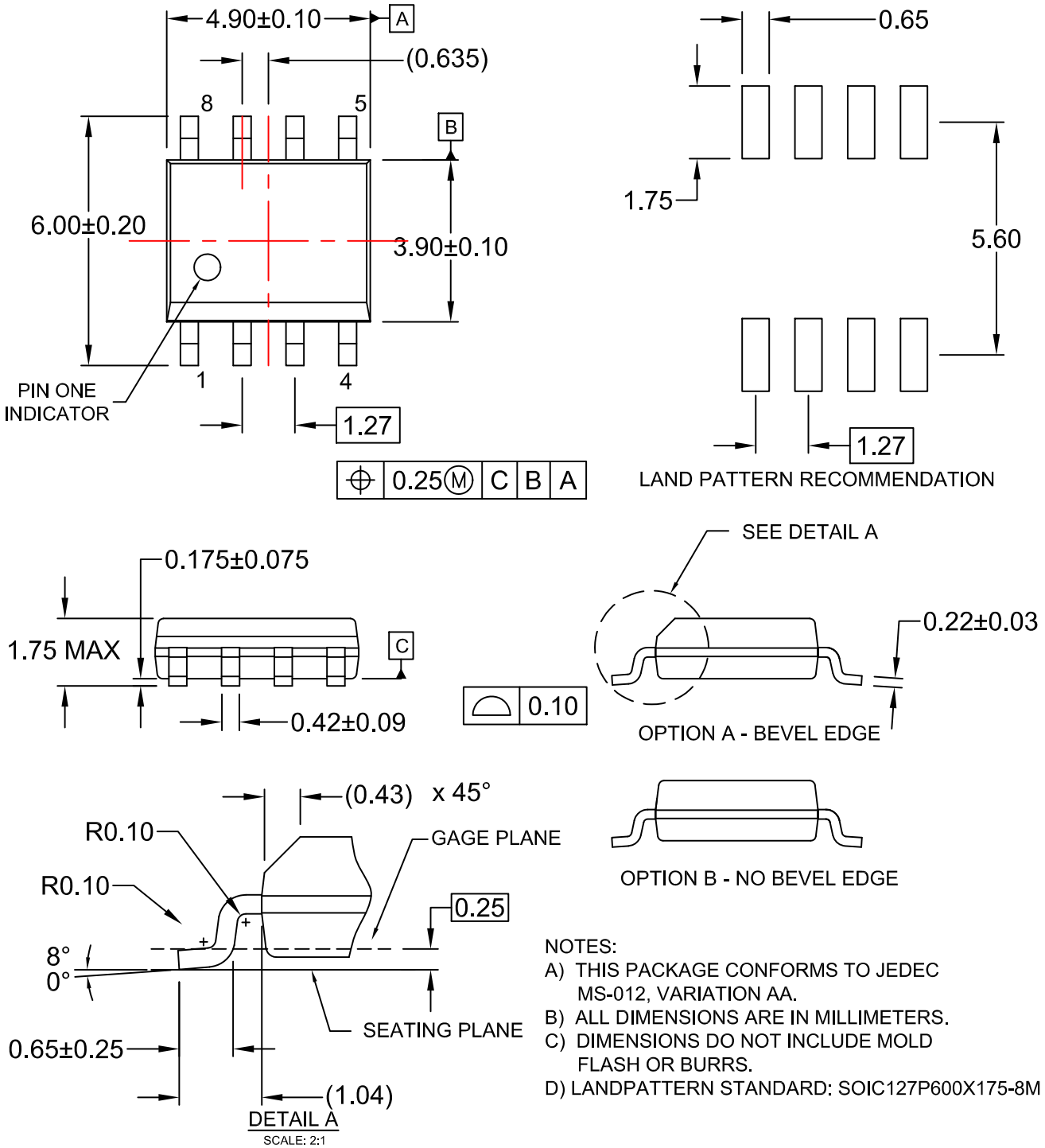

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